REMARKS

The Office Action dated June 2, 2005, has been received and carefully considered. Reconsideration of the outstanding rejections in the present application is respectfully requested based on the following remarks.

At the outset, Applicants note with appreciation the indication on page 5 of the Office Action that claims 21 and 22 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. However, Applicants have opted to defer rewriting claims 21 and 22 in independent form pending reconsideration of the arguments presented below with respect to the rejected claims.

I. THE OBVIOUSNESS REJECTION OF CLAIMS 1-4, 8-11, AND 16-20

On pages 2-5 of the Office Action, claims 1-4, 88-11, and 16-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Goldrain (U.S. Patent No. 5,742,798). This rejection is hereby respectfully traversed.

As stated in MPEP § 2143, to establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of

ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Also, as stated in MPEP § 2143.01, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). Further, as stated in MPEP § 2143.03, to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). That is, "[a]ll

words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 165 USPQ 494, 496 (CCPA 1970). Additionally, as stated in MPEP § 2141.02, a prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984). Finally, if an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Regarding claim 1, the Examiner asserts that Goldrain discloses a method for accommodating transition-induced delay comprising the steps of: determining a first relationship between a current logic state and a next logic state of a first clock signal; and adjusting a first delay of a first clock signal based at least in part upon the first relationship by controlling at least one delay element. The Examiner acknowledges that Goldrain fails to disclose that the first relationship between the current logic state and the next logic state is of a first data signal, and that a first delay of the first data signal is adjusted based at least in part upon the first relationship by controlling at least one delay element.

However, the Examiner goes on to assert that it would have been obvious to use the apparatus of Goldrain to accommodate transition-induced delay of a data signal instead of a clock signal.

Applicants respectfully disagree with the Examiner's reasoning on several points. First, it is respectfully submitted that Goldrain fails to disclose a method for accommodating transition-induced delay comprising determining a first relationship between a current logic state and a next logic state of a first data signal, as claimed. Specifically, the Examiner asserts that Goldrain discloses this claim element by determining a relationship between delayed clock 511 before and after a positive transition of reference clock 515 by providing an output 516 of flip-flop 512 (see column 4, lines 46-48; column 4 lines 66-67; and column 5, lines 1-7). However, the output 516 of flip-flop 512 does not represent a relationship between delayed clock 511 before and after a positive transition of reference clock 515. Rather, the output 516 of flip-flop 512 is merely a clocked version of the delayed clock 511 after a positive transition of reference clock 515. Indeed, Goldrain fails to disclose how any relationship is determined. Thus, Goldrain fails to disclose determining a

first relationship between a current logic state and a next logic state of a first data signal, as claimed.

Second, it is respectfully submitted that Goldrain fails to disclose a method for accommodating transition-induced delay comprising adjusting a first delay of the first data signal based at least in part upon the first relationship by controlling at least one delay element, as claimed. Specifically, the Examiner asserts that Goldrain discloses this claim element by using the output 516 of flip-flop 512 to quantify delay information that is exchanged between chips (see column 5, lines 11-12). However, Goldrain clearly does not disclose that the output 516 of flip-flop 512 is used to adjust elementary delays 502 so as to delay delayed clock 511. Rather, Goldrain clearly discloses that the output 516 of flip-flop 512 is used to provide information to another device to adjust another clock signal. Indeed, Goldrain is specifically directed to the synchronization of clock signals on different devices. Thus, Goldrain fails to disclose adjusting a first delay of the first data signal based at least in part upon the first relationship by controlling at least one delay element, as claimed.

Third, claim 1 sets forth a method for accommodating transition-induced delay in data signals. Goldrain is clearly

not directed to, nor does it even suggest, accommodating transition-induced delay in data signals, or even clock signals. Rather, Goldrain is specifically directed to the synchronization of clock signals on different devices. Also, Goldrain only discloses detecting the state of a delayed clock signal (511) on the rising edge of a reference clock signal (515) (see column 4, lines 46-48). This clearly does not amount to determining a first relationship between a current logic state and a next logic state of a first data signal, as claimed. Further, Goldrain only discloses determining the number of elementary delays (502) that are required to cause a delay of half a clock cycle of a clock signal (see column 5, lines 4-12). However, this does not amount to adjusting a first delay of the first data signal based at least in part upon the first relationship by controlling at least one delay element, as claimed. Thus, it is respectfully submitted that Goldrain does not claim, disclose, or even suggest the claimed invention. Accordingly, it is respectfully submitted that claim 1 should be allowable.

Claims 2-4 are dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claims 2-4 should also be allowable at least by virtue of their dependency on independent claim 1. Moreover, these claims recite additional features which are not claimed, disclosed, or

even suggested by the cited references taken either alone or in combination. For example, claim 2 recites determining a second relationship between a current logic state and a next logic state of a second data signal, wherein the step of adjusting the first delay of the first data signal based at least in part upon the first relationship further comprises adjusting the first delay of the first data signal based at least in part upon the first and second relationships. Nowhere does Goldrain claim, disclose, or even suggest this claimed feature. Also, claim 3 recites that the step of adjusting the first delay of the first data signal based at least in part upon the first and second relationships further comprises adjusting the first delay of the first data signal and a second delay of the second data signal based at least in part upon the first and second relationships. Nowhere does Goldrain claim, disclose, or even suggest this claimed feature. Furthermore, claim 4 recites that the step of adjusting the first delay of the first data signal based at least in part upon the first relationship further comprises providing less delay when the current logic state and the next logic state of the first data signal are different than when the current logic state and the next logic state of the first data signal are similar. Nowhere does Goldrain claim, disclose, or even suggest this claimed feature.

Regarding claim 8, the Examiner asserts that Goldrain substantially discloses the claimed invention, except that Goldrain uses clock signals instead of data signals. However, for some of the same reasons as set forth above with respect to claim 1, Applicants respectfully disagree with the Examiner's reasoning regarding claim 8 on several points. First, Goldrain is specifically directed to the synchronization of clock signals. In contrast, claim 8 sets forth an apparatus for accommodating transition-induced delay in data signals. Second, Goldrain only discloses detecting the state of a delayed clock signal (511) on the rising edge of a reference clock signal (515) (see column 4, lines 46-48). However, this does not amount to a transition detection block having a plurality of inputs for receiving a corresponding plurality of data signals, wherein the transition detection block detects transitions of the plurality of data signals, as claimed. Third, Goldrain only discloses determining the number of elementary delays (502) that are required to cause a delay of half a clock cycle of a clock signal (see column 5, lines 4-12). However, this does not amount to a delay adjustment block coupled to the transition detection block, wherein the delay adjustment block adjusts a delay in at least one of the plurality of data signals by controlling at least one delay element, as claimed. Thus, it is

respectfully submitted that Goldrain does not claim, disclose, or even suggest the claimed invention. Accordingly, it is respectfully submitted that claim 8 should be allowable.

Claims 9-11 are dependent upon independent claim 8. Thus, since independent claim 8 should be allowable as discussed above, claims 9-11 should also be allowable at least by virtue of their dependency on independent claim 8. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination. For example, claim 9 recites that the transition detection block detects a first type of the transitions from a first level to a second level and a second type of the transitions from the second level to the first level. Nowhere does Goldrain claim, disclose, or even suggest this claimed feature with respect to data signals. Also, claim 10 recites that the delay adjustment block adjusts the delay based on a relationship between the first type of the transitions and the second type of the transitions. Nowhere does Goldrain claim, disclose, or even suggest this claimed feature with respect to data signals. Further, claim 11 recites that the relationship is a difference between a first number of the plurality of data signals exhibiting the first type of the transitions and a second number of the plurality of data signals

exhibiting the second type of the transitions. Nowhere does Goldrain claim, disclose, or even suggest this claimed feature.

Regarding claim 16, the Examiner asserts that Goldrain discloses the claimed invention for the same reasons that Goldrain discloses the invention recited in claim 8. However, for the same reasons as discussed above for claim 8, it is respectfully submitted that Goldrain fails to disclose a method for accommodating transition-induced delay comprising: detecting transitions of a plurality of data signals; and adjusting a delay of at least one of the plurality of data signals based at least in part upon the transitions of the plurality of data signals by controlling at least one delay element, as claimed. Thus, it is respectfully submitted that Goldrain does not claim, disclose, or even suggest the claimed invention. Accordingly, it is respectfully submitted that claim 16 should be allowable.

Claims 17-22 are dependent upon independent claim 16. Thus, since independent claim 16 should be allowable as discussed above, claims 17-22 should also be allowable at least by virtue of their dependency on independent claim 16. Moreover, similar to claims 9-11, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claims 1-4, 8-11, and 16-20 be withdrawn.

II. CONCLUSION

In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number, in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

To the extent necessary, a petition for an extension of time under 37 CFR § 1.136 is hereby made.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-0206, and please credit any excess fees to the same deposit account.

Respectfully submitted,

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